

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	399	((laminat\$3 bond\$3) same (film plate) same (first near5 (metal condct\$3))).clm.	US-PGPU B	OR	ON	2005/12/06 14:16
L2	13220	(second near5 (condcut\$3 metal)).clm.	US-PGPU B	OR	ON	2005/12/06 14:17
L3	2311	(third near5 (condcut\$3 metal)).clm.	US-PGPU B	OR	ON	2005/12/06 14:17
L5	10086	((conduct\$3 metal) near5 wir\$3).clm.	US-PGPU B	OR	ON	2005/12/06 14:19
L6	42677	(IC die chip).clm.	US-PGPU B	OR	ON	2005/12/06 14:19
L7	75193	(insulat\$3 dielectric).clm.	US-PGPU B	OR	ON	2005/12/06 14:20
L8	176527	(etch\$3 expos\$3 remov\$3).clm.	US-PGPU B	OR	ON	2005/12/06 14:20
L9	47594	(electrical\$3 near5 connect\$3).clm.	US-PGPU B	OR	ON	2005/12/06 14:20
L10	2	1 and 2 and 3 and 5 and 6 and 7 and 8 and 9	US-PGPU B	OR	ON	2005/12/06 14:23

L11	2	((laminat\$3 same first conductive same second conductive same film same third same conductive) and(conductive same wiring same layer same etching same first same conductive same film) and (removing same third same conductive same film same conductive same wiring same layer same mask) and (third same conductive same film same conductive same wiring same layer) and (exposing same conductive same wiring layer same insulating layer same fitting same semiconductor same elements) and (electrically same connecting same semiconductor same elements same conductive same wiring same layer) and (sealing same resin same layer) and (removing same second conductive same film same third same conductive same rear surface)".clm"	US-PGPU B	OR	ON	2005/12/06 14:33
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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	56041	(conduct\$3 wir\$3) same mask same (expos\$3 remov\$3 etch\$3 pattern\$3)	US-PGPU B; USPAT; USOCR	OR	ON	2005/12/06 14:00
L2	11379	L1 and ((IC die chip) same (connect\$3 fitt\$3))	US-PGPU B; USPAT; USOCR	OR	ON	2005/12/06 14:00
L3	7818	L2 and (electrical\$3 near5 connect\$3)	US-PGPU B; USPAT; USOCR	OR	ON	2005/12/06 14:00
L4	6897	L3 and (insulat\$3 dielectric)	US-PGPU B; USPAT; USOCR	OR	ON	2005/12/06 14:01
L5	3141	L4 and resin	US-PGPU B; USPAT; USOCR	OR	ON	2005/12/06 13:56
L6	1897	L5 and (first near5 (metal conductive))	US-PGPU B; USPAT; USOCR	OR	ON	2005/12/06 13:57
L7	1578	L6 and (second near5 (metal conductive))	US-PGPU B; USPAT; USOCR	OR	ON	2005/12/06 13:57
L8	644	L7 and (third near5 (metal conductive))	US-PGPU B; USPAT; USOCR	OR	ON	2005/12/06 13:58
L9	636	8 and (etch\$3 pattern\$3)	US-PGPU B; USPAT; USOCR	OR	ON	2005/12/06 13:58
L10	21908	(conduct\$3 wir\$3) same mask same (expos\$3 remov\$3 etch\$3 pattern\$3)	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/12/06 14:00
L11	488	L10 and ((IC die chip) same (connect\$3 fitt\$3))	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/12/06 14:00
L12	139	L11 and (electrical\$3 same connect\$3)	EPO; JPO; DERWENT ; IBM_TDB	OR	ON	2005/12/06 14:01

L13	70	L12 and (insulat\$3 dielectric)	EPO; JPO; <b>DERWENT</b> ; IBM_TDB	OR	ON	2005/12/06 14:01
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